IN THE CLAIMS

1. (Amended) An apparatus for converting data between serial and parallel formats, comprising:

at least one serial data channel [(20),];

a storage element [(30)]associated with each said serial data channel [(20)]and having at least first and second arrays [(31, 32)]of storage cells[(50, 50')],[**characterised in that]** wherein each said storage cell [comprises] includes first and second ports, wherein the first ports of all storage cells [(50, 50')]of a storage element [(30)]are connected in parallel to a data bus [(60)]interconnecting the storage element [(30)]with [the]an associated channel[(20)], and wherein the data bus [(60)]comprises at least one buffering element [(70)]arranged to separate said data bus into portions[(61-64)], each of said portions being connected to the first port of at least one of said storage cells[(50, 50')] of each array[(31, 32)] of said storage element[,]; and

means [(100; 300) are provided]for enabling[the transfer of] data transfer between said bus[(60)] and at least one of said storage cells[(50, 50') in said storage element (30)] via a corresponding one of said first ports, and for enabling[the transfer of] data transfer from at least one of said[one bus (61-64)] portions to an adjacent[bus] portion via said at least one buffering element[(70)].

2. (Amended) An apparatus as claimed in claim 1, [**characterised in that**]wherein said means [(100: 300)] for enabling[the transfer of] data transfer [between said bus (60) and one storage cell (50, 50')] comprises first clock generating means[, said first clock being] adapted to control access to said storage cells[(50,50')] and to control the data transfer[of data from one bus portion (61-64)] to the adjacent portion[next via said buffering element (70)].

3. (Amended) An apparatus as claimed in claim 2, [**characterised in that**]wherein said first clock generating means is adapted to[the] a transmission speed [of the]corresponding to an associated said serial data channel[(20)].

4. (Amended) An apparatus as claimed in any preceding claim, [**characterised in that**]wherein the first ports of the storage cells[(50, 50')] of each of said arrays[(31, 32)] are adapted to be accessed sequentially.

5. (Amended) An apparatus as claimed in[any preceding] claim 1, [**characterised in that**]wherein said buffering element includes at least one side, and for[in] each of said arrays, the first ports of the storage cells[(50, 50')] are disposed on each side of [a]the buffering element[(70)] and are adapted to be accessed simultaneously.

6. (Amended) An apparatus as claimed in[any preceding] claim 1,[**characterised in that**] wherein said buffering element[(70)] comprises a pipeline register.

7. (Amended) An apparatus as claimed in[any preceding] claim 1,[**characterised in that**] wherein the second ports of each of said storage cells[(50, 50')] are connected in parallel across all of said arrays.

8. (Amended) An apparatus as claimed in[any preceding] claim 2,[**characterised in that**] further comprising means[(200; 400) are provided] for controlling[the] access to the storage cells[(50, 50')] of one of said array simultaneously via said second ports.

9. (Amended) An apparatus as claimed in claim 8,[**characterised in that**] wherein said means[(200:400)] for controlling[the] access to the storage cells comprises a second clock generating means.

10. (Amended) An apparatus as claimed in[any preceding] claim 1,[**characterised in that**] wherein said storage cells[(50, 50')] comprise dual-port random access memory (RAM) cells.

11. (Amended) An apparatus as claimed in[any preceding] claim 1,[**characterised in that**] wherein each of said arrays[(31, 32)] is[dimensioned] adapted to store at least one data packet.

12. (Amended) An apparatus as claimed in[any one of] claim[s] 1[to 10],[**characterised in that**] wherein each of said arrays[(31, 32)] is[dimensioned] adapted to store part of a data packet.

13. (Amended) An apparatus as claimed in[any preceding] claim 1,[**characterised in that**] wherein said storage cells[(50, 50')] are arranged to store more than one bit of data simultaneously.

14. (Amended) An apparatus[for converting] as claimed in claim 1, wherein said data is converted from a serial to parallel format[as claimed in any preceding claim, **characterised in that**] and wherein said first ports[is] are[a] input ports and said second ports[is an] are output ports.

15. (Amended) An apparatus[for converting] as claimed in claim 1, wherein said data is converted from a parallel to serial format[as claimed in any one of claims 1 to 12, **characterised in that**] and wherein said first ports[is an] are output ports and said second ports[is an]are input ports.

16. (Amended) An apparatus for converting data input through at least one channel in a serial format into a parallel format, comprising:

at least one serial data input channel[(20),];

a storage element[(30)] associated with each said serial data channel[(20)] and having at least first and second arrays[(31, 32)] of storage cells[(50, 50')],[**characterised in that**] wherein each of the storage cells[(50, 50')] [comprises] includes an input port and an output port, [the]such that input ports for all of the storage cells of the storage element[(30) being] are connected in parallel to a data bus[(60)] interconnecting the storage element[(30)] with an

associated serial data channel[(20)], and wherein said data bus[(20)] comprises at least one buffering element[(70)] arranged to separate said data bus into portions[(61-64)], each of said portions being connected to an[the] input port of at least one of said storage cells[(50, 50')] of each array of said storage element[,]; and

means[(100) are provided] for enabling[the] data input[of data] from said data bus [in]to at least one of said storage cells[(50, 50')] in said storage element[(30)] and for enabling said buffering element to[the] buffer[ing of] said data onto [a]said data bus portion[(61-64) by said at least one buffering element (70)] in accordance with a predetermined input cycle.

17. (Amended) An apparatus for converting data from a parallel format into a serial format, comprising:

at least one serial data output channel[(20),];

a storage element[(30)] associated with each said serial data output channel[(20)] and having at least first and second arrays[(31, 32)] of storage cells[(50, 50'), **characterised in that**], each of the storage cells[(50, 50') comprises] including an input port and an output port, such that[the] output ports for all of the storage cells[(50, 50')] of the storage element[(30) being] are connected in parallel to a data bus[(60)] interconnecting the storage element with an associated serial data output channel[(20)], and wherein said data bus[(60)] comprises at least one buffering element[(70)] arranged to separate said data bus into portions[(61-64)], each of said portions being connected to an[the] output port of at least one of said storage cells[(50, 50')] of each array of said storage element[(30),]; and

means[(300) are provided] for enabling[the] data output[of data] from at least one of said storage cells[(50,50')] in said storage element[(30)] onto said data bus[(60)] and for enabling said buffering element to the buffer[ing of] said data onto[a] data bus portion[(61-64) by said at least one buffering element (70)] in accordance with a predetermined output cycle.

18. (Amended) ~~A method~~ apparatus for converting serial data to a parallel format utilising[the] an apparatus as claimed in any one of claims 1 [to 14 and]or 16, [**characterised by**]said method comprising the steps of:

transmitting serial data from each said channel[(20)] onto the [associated]said data bus [(60)]associated therewith, and

enabling[the] sequential input of data from the data bus[(60)] into the [memory]storage cells[(50,50')] of a corresponding one of said arrays[(31, 32) of] for each said storage element[(30)] in accordance with a write cycle.

19. (Amended) A method as claimed in claim 18,[**characterised by** enabling the] further comprising the step of, simultaneous with the step of enabling sequential input of data, outputting[of] data from the [memory]storage cells[(50,50')] of [one]the other of said arrays[(31, 32) of] for each storage element[(30)] sequentially and in accordance with a read cycle[, the arrays (31, 32) in which data output and data input are enabled being different].

20. (Amended) A method as claimed in claim [18]19,[**characterised by**] further comprising the step of splitting the outputting of data from the [memory]storage cells[(50,50') of one array (31, 32)] over at least two read cycles.

21. (Amended) A method as claimed [in any one of] claim[s] 18 to [20, **characterised by**] further comprising the step of enabling[the] data transfer[of data] from one of said bus portions[(61-64)] to an adjacent[following] bus portion during each said write cycle.

22. (Amended) A method as claimed in claim 21,[**characterised by**] further comprising the step of commencing the sequential input of data into each of said arrays[(31, 32)] from one of the portions[of data bus (64)] arranged furthest from[the] an associated serial data channel[(20)].

23. (Amended) A method as claimed in claim 22,[**characterised by**] further comprising the step of enabling the sequential input of data to the storage cells[(50,50')] at[the] an end of one of said bus portions[(61-64)] and at a[the] beginning of[the]a next bus portion simultaneously.

24. (Amended) A method as claimed in[any one of] claim[s] 18[to 23],[**characterised by**] further comprising the step of adapting the write cycle for each said storage element[(30)] to[the] be at a transmission speed of [the]an associated serial data channel[(20)].

25. (Amended) A method as claimed in claim[24, **characterised by**] 19, further comprising the step of adapting the read cycle to [the]correspond to a total bandwidth of [all serial data]every said channel[s (20)].

26. (Amended) A method for converting parallel data to a serial format utilising[the] an apparatus as claimed in ~~any one of~~ claims 1[to 13, 15 and] or 17, [**characterised by**]said method comprising the steps of:

enabling the sequential output of data from the [memory]storage cells[(50,50')] of one of said arrays[(31, 32) of] for each storage element[(30)] onto the data bus[(60)] in accordance with a read cycle; and

transmitting serial data from[each]the data bus[(60)] onto the [associated]serial data channel [(20)]associated therewith.

27. (Amended) A method as claimed in claim 26,[**characterised by** enabling the] further comprising the step of, simultaneous with the step of enabling the sequential output of data, inputting[of] data into the memory cells[(50,50')] of [one]the other of said arrays[(31, 32) of] for each storage element[(30)] sequentially and in accordance with a write cycle[, the arrays (31, 32) in which data output and data input are enabled being different].

28. (Amended) A method as claimed in claim[26 or] 27,[**characterised by**] further comprising the step of splitting the inputting of data into the [memory]storage cells[(50,50')] of one array[(31, 32)] over at least two write cycles.

29. (Amended) A method as claimed in[any one of] claim[s] 26[to 28],[**characterised by**] further comprising the step of enabling[the] data transfer[of data] from one of said bus portions[(61-64)] to an adjacent[following] bus portion during each said write cycle.

30. (Amended) A method as claimed in claim 29,[**characterised by**] further comprising the step of commencing the output of data from each of said arrays[(31, 32)] onto one of the portions[of data bus] arranged closest to [the]an associated serial data channel[(20)].

31. (Amended) A method as claimed in claim 30,[**characterised by**] further comprising the step of enabling the sequential output of data from the storage cells[(50,50')] at[the] an end of one of said bus portions[(61-64)] and[the] at a beginning of [the]a next bus portion simultaneously.

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32. (Amended) A method as claimed in[any one of] claim[s] 26[to 31],[**characterised by**] further comprising the step of adapting the read cycle for each said storage element[(30)] to [the]be at a transmission speed of [the]an associated serial data channel[(20)].

33. (Amended) A method as claimed in claim [32, **characterised by**]27, further comprising the step of adapting the write cycle to [the]correspond to a total bandwidth of [all serial data]every said channel[s (20)].

34. (Amended) A communications switch comprising an apparatus as claimed in any one of claims 1[to], 16 or 17.

35. (Amended) A communications switch as claimed in claim 34,[**characterised in that**] wherein said apparatus operates in accordance with a method as claimed in any one of claims 18 [to 33]or 26.